

Application number 10/796,500  
Amendment dated April 17, 2006  
Reply to office action of October 17, 2005

PATENT

**Amendments to the Specification:**

Please replace paragraph 0006 with the following amended paragraph:

[0006] According to one embodiment, a programmable hysteretic amplifier of the present invention can be used as an input buffer for an input signal applied to an input pin of an integrated circuit. According to another embodiment, three programmable hysteretic amplifiers of the present invention are coupled together to provide improved sensing of small differential input voltages. The first two amplifiers receive the input signals. Outputs of these two amplifiers drive the inputs of the third amplifier.

Please replace paragraph 0022 with the following amended paragraph:

[0022] Figure 2 illustrates a schematic of a first embodiment of a programmable hysteretic amplifier 200 of the present invention. As with Figure 1, IN and INB are the in-coming differential input signals. Amplifier 200 amplifies the ~~different~~ difference between the input signals to ~~drives~~ drive output signal OUT. Amplifier 200 can be used as a comparator that drives OUT to a high or a low logic state. Amplifier 200 includes a differential amplifier stage 201, a multiplexer 202, and two inverters 203-204.

Please replace paragraph 0025 with the following amended paragraph:

[0025] The voltage controls signals DIS and HSEL control the hysteretic input threshold voltages of amplifier 200. When DIS is set to a high voltage, the amplifier has only one input voltage threshold and therefore has no hysteresis. When DIS is low and HSEL is high, amplifier 200 has positive hysteresis. When DIS is low and HSEL is low, amplifier 200 has negative hysteresis. Dynamic hysteretic amplifiers of the present invention can be programmed with positive hysteresis to filter out input noises or with negative hysteresis to speed up data transmission.

Please replace paragraph 0034 with the following amended paragraph:

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[0034] Even when the input voltage IN equals voltage INB, voltage VR is lower than the voltage at VL, due to the extra current path through the ~~transistor~~ transistors 224 and 226. Therefore, the output voltage OUT is still held at a stable value. The output voltage OUT is held low until the voltages IN and INE reach a first hysteretic threshold (point B on the waveforms in Figure 3B). Because both transistors 221-222 always have the same control gate voltages, they both have the same drain-source current.